AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A semiconductor integrated circuit device comprising:

~~a predetermined~~ plural I/O cells provided in an I/O area in a peripheral portion of a chip ~~and~~, said I/O cells being arranged to be connected to external pins;

signal wirings which transfer a test signal to said I/O cells and are provided in said I/O area in a layout direction of said ~~plurality of~~ I/O cells; and

~~at least one empty cell where said signal wirings run and which is to be a transfer path for said test signal, is provided in said I/O area and has a repeater circuit that receives said test signal and outputs said test signal~~ plural repeater circuits that are each in a different part of said I/O area that does not include one of said I/O cells and through which said signal wirings run, each of said repeater circuits receiving and outputting said test signal and being optimized in electrical characteristics for a delay condition for a location thereof.

2. (canceled)

3. (original) The semiconductor integrated circuit

device according to claim 1, wherein said I/O cells include a boundary-scan register circuit and said signal wirings include a wiring for a signal to be supplied to said boundary-scan register circuit.

4. (original) The semiconductor integrated circuit device according to claim 3, wherein said I/O cells include a scan flip-flop circuit for a scan path test and said signal wirings include a wiring for a scan path test signal to be supplied to said scan flip-flop circuit.

5. (currently amended) A design automation apparatus for a semiconductor integrated circuit, comprising:

a memory unit which stores I/O cell layout position information, I/O cell size information, I/O cell test terminal information, technology information including design information, and information on a repeater circuit to be laid out in an empty cell for each type of I/O ~~cells~~ cell on a chip which are to be connected to external pins;

a computing section which computes a wiring length of a sub net between adjoining I/O cells for test signals (called "test net") to be connected to an area for layout of I/O cells (called "I/O area") at a peripheral portion of a chip by referring to said I/O cell layout position information, I/O cell size information and I/O cell test terminal information in said memory unit and outputs said wiring length;

a circuit simulator;

a determining section which computes information at least on a wiring resistance and a capacitance for said sub net, causes said circuit simulator to execute circuit simulation to acquire a wiring delay of said sub net and waveform depression at an end of said sub net, and determines an optimal repeater circuit to be inserted in an empty cell where said sub net passes, based on said information on said repeater circuit stored in said memory unit in case where said wiring delay and waveform depression concerning said sub net are out of a predetermined range of allowance defined in said technology information; and

a layout section which lays out an empty cell including said determined repeater circuit in said I/O area.

6. (currently amended) The design automation apparatus according to claim 5, wherein said determining section which determines a repeater circuit includes a control section which executes a circuit simulation for a sub net divided by insertion of a selected repeater circuit to acquire a wiring delay and waveform depression concerning said divided sub net, determines whether said wiring delay and waveform depression concerning said divided sub net fall within said range of allowance defined in said technology information or not, and searches for an ~~optical~~ optimal repeater circuit by selecting another repeater circuit or further dividing said sub net in case where said wiring delay and waveform depression do not fall within said range of allowance.

7. (currently amended) A design automation method for a

semiconductor integrated circuit using a computer having a memory unit which stores I/O cell layout position information, I/O cell size information, I/O cell test terminal information, technology information including design information, and information on a repeater circuit to be laid out in an empty cell for each type of I/O ~~cells~~ cell on a chip which are to be connected to external pins, said method comprising the steps of:

computing a wiring length of a sub net between adjoining I/O cells for test signals (called "test net") to be connected to an area for layout of I/O cells (called "I/O area") at a peripheral portion of a chip by referring to said I/O cell layout position information, I/O cell size information and I/O cell test terminal information in said memory unit and outputting said wiring length;

computing information at least on a wiring resistance and a capacitance for said sub net, causing ~~said~~ a circuit simulator to execute circuit simulation to acquire a wiring delay of said sub net and waveform depression at an end of said sub net;

determining an optimal repeater circuit to be inserted in an empty cell where said sub net passes, based on said information on said repeater circuit stored in said memory unit in case where said wiring delay and waveform depression concerning said sub net are out of a predetermined range of allowance defined in said technology information; and

laying out an empty cell including said determined repeater circuit in said I/O area.

8. (currently amended) The design automation method according to claim 7, wherein said step of determining a repeater circuit includes the steps of:

performing control in such a way as to execute circuit simulation for a sub net divided by insertion of a selected repeater circuit to acquire a wiring delay and waveform depression concerning said divided sub net; and

determining whether said wiring delay and waveform depression concerning said divided sub net fall within said range of allowance defined in said technology information or not, and searching for an ~~optical~~ optimal repeater circuit by selecting another repeater circuit or further dividing said sub net in case where said wiring delay and waveform depression do not fall within said range of allowance.

9. (currently amended) A program ~~for allowing~~ embodied in a computer-readable medium causing a computer having a memory unit which stores I/O cell layout position information, I/O cell size information, I/O cell test terminal information, technology information including design information, and information on a repeater circuit to be laid out in an empty cell for each type of I/O ~~cells~~ cell on a chip, which are to be connected to external pins, to execute:

a first process of computing a wiring length of a sub

net between adjoining I/O cells for test signals (called "test net") to be wired to an area for layout of I/O cells (called "I/O area") at a peripheral portion of a chip by referring to said I/O cell layout position information, I/O cell size information and I/O cell test terminal information in said memory unit and outputting said wiring length;

a second process of computing information at least on a wiring resistance and a capacitance for said sub net, causing ~~said~~ a circuit simulator to execute circuit simulation to acquire a wiring delay of said sub net and waveform depression at an end of said sub net;

a third process of determining an optimal repeater circuit to be inserted in an empty cell where said sub net passes, based on said information on said repeater circuit stored in said memory unit in case where said wiring delay and waveform depression concerning said sub net are out of a predetermined range of allowance defined in said technology information; and

a fourth process of laying out an empty cell including said determined repeater circuit in said I/O area.

10. (currently amended) The program according to claim 9, wherein in said third process, said computer executes:

a process of performing control in such a way as to execute circuit simulation for a sub net divided by insertion of a selected repeater circuit to acquire a wiring delay and waveform depression concerning said divided sub net; and

a process of determining whether said wiring delay and waveform depression concerning said divided sub net fall within said range of allowance defined in said technology information or not, and searching for an ~~optical~~ optimal repeater circuit by selecting another repeater circuit or further dividing said sub net in case where said wiring delay and waveform depression do not fall within said range of allowance.

11. (new) A semiconductor integrated circuit device comprising:

predetermined I/O cells provided in an I/O area in a peripheral portion of a chip and to be connected to external pins;

signal wirings which transfer a test signal to said I/O cells and are provided in said I/O area in a direction along which I/O cells are provided; and

at least one empty cell where said signal wirings run and which is to be a transfer path for said test signal, is provided in said I/O area and has a repeater circuit that receives said test signal and outputs said test signal wherein the empty cell is not connected to the external pin.

12. (new) The semiconductor integrated circuit device according to claim 11, further comprising an optimal repeater circuit that has a characteristic which satisfies a delay condition for at least a predetermined signal and that is selected from plural types of repeater circuits different from

one another in electric characteristics previously prepared for one empty cell or a plurality of empty cells in said I/O area and that is laid out in said one empty cell or said plurality of empty cells as said repeater circuit for said empty cell.

13. (new) The semiconductor integrated circuit device according to claim 11, wherein said I/O cells include a boundary-scan register circuit and said signal wirings include a wiring for a signal to be supplied to said boundary-scan register circuit.

14. (new) The semiconductor integrated circuit device according to claim 13, wherein said I/O cells include a scan flip-flop circuit for a scan path test and said signal wirings include a wiring for a scan path test signal to be supplied to said scan flip-flop circuit.